Notice of Allowability	Application No.	Applicant(s)	
	10/663,612	DRIEDIGER, STEVEN	
	Examiner	Art Unit	
	Esaw T. Abraham	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Amdt filed on 06/11/06*.

2. ☒ The allowed claim(s) is/are *1-38*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

GUY LAMARRE
PRIMARY EXAMINER

DETAILED ACTION

Examiner's statement for reason for allowance

1. Claims 1-15 have been allowed.

Claims 16-37 have been previously allowed.

Examiner's statement for reason for allowance

2. Claims **1-15** have been allowed.

The following is an examiner's statement for allowance:

As per claim 1:

The prior art of record, Quach et al. (U.S. PN: 6,654,909) teaches an error detection apparatus is used to periodically read out the critical resources and compute their parity or ECC bits. The parity and ECC bits may be shared within the same or across the critical resources. In the TLB pre-validated RIDs or protection keys case, because the RIDs and/or the data are updated relatively infrequently, this scheme provides good protection against soft errors (see col. 2, lines 10-18). Further in figure 1 Quach et al. disclosed an error detection apparatus being used to protect pre-validated region identifications (RIDs) in the translation look aside buffer (TLB), a simple 1-bit parity scheme is used by an error detection apparatus 100 to protect a pre-validated RID array 145 in a TLB 140. The TLB 140 includes the RID array 145, a RID parity bit array 146, a protection key register array 150, a protection Key register parity bit array 151, an enable/disable bit 155, a virtual address 160 and a physical address 165 (see col. 2 lines 52-67).

The prior art of record, Ichiriu (U.S. PN: 6,597,595) in figure 25 discloses a CAM device (700) includes an error CAM (715) to assert a match error signal (732) if a match index (174) matches any of a plurality of error addresses. In addition to the error CAM, the CAM device includes an address circuit (103), comparand register (115), and error detection circuit (711). Further, the address circuit, comparand register is coupled to one another and operates generally. Furthermore, an error detection circuit (711), for example, by the parity check circuit (201) and logic gate (222) described above in reference to FIG. 6 is coupled to receive the selected CAM word and output an error signal (712) to the error CAM (715). The error detection circuit asserts the error signal upon detecting an error in the selected CAM word and deasserts the error signal if no error is detected (see col. 24, lines 10-41). However, the prior arts taken singly or in combination fail to teach, anticipate, suggest, or render obvious a method for detecting data errors associated with a Content Addressable Memory (CAM) module, comprising comparing the predetermined protection word with the key-based protection word for facilitating issuance of an output error indication when the predetermined protection word is different than the key-based protection word. Consequently, claim 1 is allowed over the prior art.

Claims **1-10,** which is/are directly or indirectly dependent/s of claim 16 are also allowable over the prior art of record.

As per claim 12:

The prior art of record, Quach et al. (U.S. PN: 6,654,909) teaches an error detection apparatus is used to periodically read out the critical resources and compute their parity

or ECC bits. The parity and ECC bits may be shared within the same or across the critical resources. In the TLB pre-validated RIDs or protection keys case, because the RIDs and/or the data are updated relatively infrequently, this scheme provides good protection against soft errors (see col. 2, lines 10-18). Further in figure 1 Quach et al. disclosed an error detection apparatus being used to protect pre-validated region identifications (RIDs) in the translation look aside buffer (TLB), a simple 1-bit parity scheme is used by an error detection apparatus 100 to protect a pre-validated RID array 145 in a TLB 140. The TLB 140 includes the RID array 145, a RID parity bit array 146, a protection key register array 150, a protection Key register parity bit array 151, an enable/disable bit 155, a virtual address 160 and a physical address 165 (see col. 2 lines 52-67).

The prior art of record, Ichiriu (U.S. PN: 6,597,595) in figure 25 discloses a CAM device (700) includes an error CAM (715) to assert a match error signal (732) if a match index (174) matches any of a plurality of error addresses. In addition to the error CAM, the CAM device includes an address circuit (103), comparand register (115), and error detection circuit (711). Further, the address circuit, comparand register is coupled to one another and operates generally. Furthermore, an error detection circuit (711), for example, by the parity check circuit (201) and logic gate (222) described above in reference to FIG. 6 is coupled to receive the selected CAM word and output an error signal (712) to the error CAM (715). The error detection circuit asserts the error signal upon detecting an error in the selected CAM word and deasserts the error signal if no error is detected (see col. 24, lines 10-41). However, the prior arts taken singly or in combination fail to teach, anticipate, suggest, or render obvious a method for detecting data errors associated with a Content Addressable Memory (CAM) module, comprising and

comparing the predetermined protection word with the key-based protection word for determining whether the predetermined protection word is the same as the key-based protection word. Consequently, claim 12 is allowed over the prior art.

Claims 13-15, which is/are directly or indirectly dependent/s of claim 12 are also allowable over the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned (571) 273-8300.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have

questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

Art unit: 2133

GUY LAMARRE
PRIMARY EXAMINER